## TSO?Total Store Ordering?????

1. TSO Total Store Ordering					
2.	X86 RISC-V T	SO <sub>III</sub>	RVTSO	x86 <u>□</u>	TSO
	Intel AMD				
3.	3. x86── SC── sequential consistency───── FIFO□ writ				buffer
4.	TSO[] SC[[[[[]]]] store[[[[]]]	write	buffer	load□ bypass	
	1 SC				
	2.	memory	/ consistency		
5.	☐ TSO  store-load  store-	I	FENCE FENCE		
			FENCE	write buffer <u></u>	FENCE
	□□□□□□□□ load□□□				

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