acquire release ???????

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1. □□□□□□□□ CPU □□□□□ □□□□□ **Program Order**□
   □□
   □□□□□□□□□□□□
   1. □□ CPU□□□□□□□□□□ scoreboard□□□□□□ data hazard□ address hazard
      □□□□□□□□□□□□□□□□□□□□□□□□ CPU□□□□□□□□□
2. □□ □□□□□□□□□ **multi-hart**□□□
   □□□□□□□□□□□□□□□□□□□□□□□□□□
   1. □□□□□ Out-of-Order Execution□
   2. □□□□□ Cache Hierarchy□□
   3. □□□□□□ Store Buffer□ **□ **CPU□□□□□□□ cache□ in-flight□□□□□
   4. □□□□□□□□□□□□□□□□□□□□□□□□□□□□□
   5. □□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□ **“□
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      1. □□□ 1□□□□ “□ ”□□□□□□□□ “□ ”□□□□□□□□□□□□
      2. □□□□□□ -□□□□□□□ 2□□□□□ “□ ”□□□□□□□
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         □
   6. □□□□□□ “□□□□ ”□□□□□ “□ ”□□□□ “□ ”
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3. □□□□□□□ **“□□□□ ”**□□□□□ CPU □□□□□□□□□□□□
   1. □□ `acquire`□ `releasey`□□□□□□□□□□□ LR.W □ SC.W
      □□□□□□□□□□□□□□□□□□□□□□□□ LR.W □ SC.W
      □□□□□□□□□□□□□□
   2. □□□□ LR.W □ SC.W □□□□□□□□□□□□□□□□□□□□□□□□□□□□□
4. □□□□
   1. □□□□□□□□□□□□□□□□□□□□□□□□□
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`LR.W`(Load-Reserved)??

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1. □□□ □□□□□□ `rs1`□□ 32□□□□□□□ `rd`□
2. □□□□□□ □
   - □□□□□□□□ L1 Cache□□□□□□□□ **Reserved**□□□□□□□
   - □□□□□□□□□□ Hart□□□□□□□□□□□□

3. □□ **acquire**□□ □□□□□□□□□
   - □□□□□□□□□□□□□□ `LR.W`□□□□□□□□□□□□□□□□

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- □□□□□□□□ □
  - □□□□□□□□□□□□□ **Reservation Register**□□□□□□□□□□□□□□□□□□□ ID□
  - □□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□ Invalidate□□

?? `SC.W`**(Store-Conditional)?**?

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1. □□□□□□□ □
   - □□□ `rs1`□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□
     - □□□□□□□ `rs2`□□□□ `rs1`□
     - □□□□□□□□
     - □ `rd`□□ `0`□□□□□□
   - □□□□□□□□□□□□□□□□□□□□ `rs1`□□
     - □□□□□□
     - □ `rd`□□ `□0□`□□□□ 1□□□□□
2. □□ **release**□□ □□□□□□□□□
   - □□□□□□□□□□□□□□□□ `SC.W`□□□□□□□□□□□□□□□□□□□

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- □□□□ □
  - □□□□□ **Atomic Write** □□□□□
  - □□□□□□□□□□□

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```
# □□□□□aq/rl□□□□□□□□
lock:
  lr.w.aq t0, (a0)       # □acquire□□□□□
  bnez    t0, lock       # □□□□□□□□□t0!=0□□□□
  li      t1, 1
  sc.w.rl t0, t1, (a0)   # □release□□□□□
```

```
  bnez    t0, lock       # □□□□□□t0!=0□□□□

# □□
unlock:
  sw.rl   zero, (a0)     # □release□□□□□□□
```

?????????

```
Core 0                          Core 1
======                          ======
1. lr.w t0, (x)                3. lr.w t0, (x)
   - □□x=0□□□□□□□□           - □□x=0□□□□□□□□
2. sc.w t1, 1, (x)             4. sc.w t1, 1, (x)
   - □□□□□□□□□□□x=1□       - □□□□□□□□Core 0□□x□□□□□□
   - t1=0                          - t1=1
```

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