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1. 
2. 
3. N to N 
4. 
5.  pulling  latency
6. 
1. transformer  Flash-attention  L1  fusion  DMA 
7. 

Global

1. 
2. 
3. 
  1. DMA  Kernel 
4. 

[illegible]

1. Sync mailbox N to N
2. producer consumer Pipeline
- 3.
- 1.
- 2.
- 4.
- 5.
1. write mbx wait mbx
- ack latency

[illegible]

## mbarrier

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1. [16 blocks] M barrier [3 blocks]
1. [4 blocks]
2. [12 blocks]
2. [8 blocks]
1. [32 blocks]
- [1 block]
2. [6 blocks] fence

3. ☐ Core0 Store()    Core0 Fence()    memory Ack()    Core0 Signal(Core1 mbx)
  4. ☐ Core0 Store\_mbarrier()    Core1 Wait(mbarrier)
  3. ☐
    1. ☐
  4. ☐
    1. ☐    wait☐    local☐    mbarrier☐    counter☐    latency☐
    2. ☐    transaction☐
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Revision #2

Created 11 January 2025 02:47:33 by Colin

Updated 15 January 2025 03:25:09 by Colin