

????

- 

??????

??python????module???










1. python[ ] module[ ]
2. [ ] latch[ ]
3. [ ] module[ ]
4. [ ]

??throughput?latency???













1. [ ] inst
2. [ ] TL throughput latency[ ] Module
  1. [ ] thread [ ]
  2. [ ] inst latency
  3. [ ] inst throughput[ ]
  4. [ ] stand-by[ ]
3. TL[ ]
4. TL[ ] python[ ] inst[ ]
5. [ ] Module
6. TL[ ] time line[ ]

????????????????






1. [ ]
2. [ ] throughput[ ] latency[ ]
3. [ ]
4. [ ]
5. [ ]
6. [ ]
  1. [ ]
  2. [ ]
  3. [ ]
7. flow plan Place and router [ ]
  1. [ ]
  2. [ ]
  3. [ ]
    1. [ ]

2. 
3.  1 
4.  2 
5.  3  1  2 

?????

1. 
2.   

  1.  /credit/valid
  2.  bank  structure harz
  3. RAW  WAW  Data harz
  4.  cache line
  5. 
3. 
  1. 

?????????Logicsim

1.  Latch
2.  Launch
3.  Status
  1. ISA/UIISA  module 
  2. 